

FIG. 1

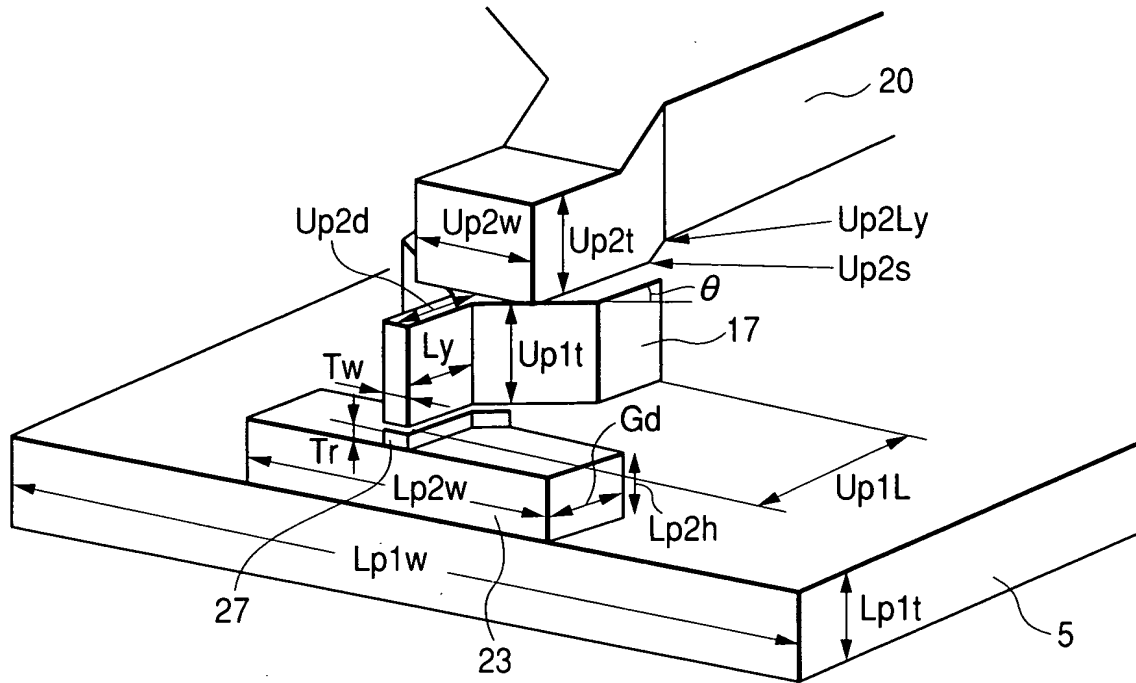


FIG. 2

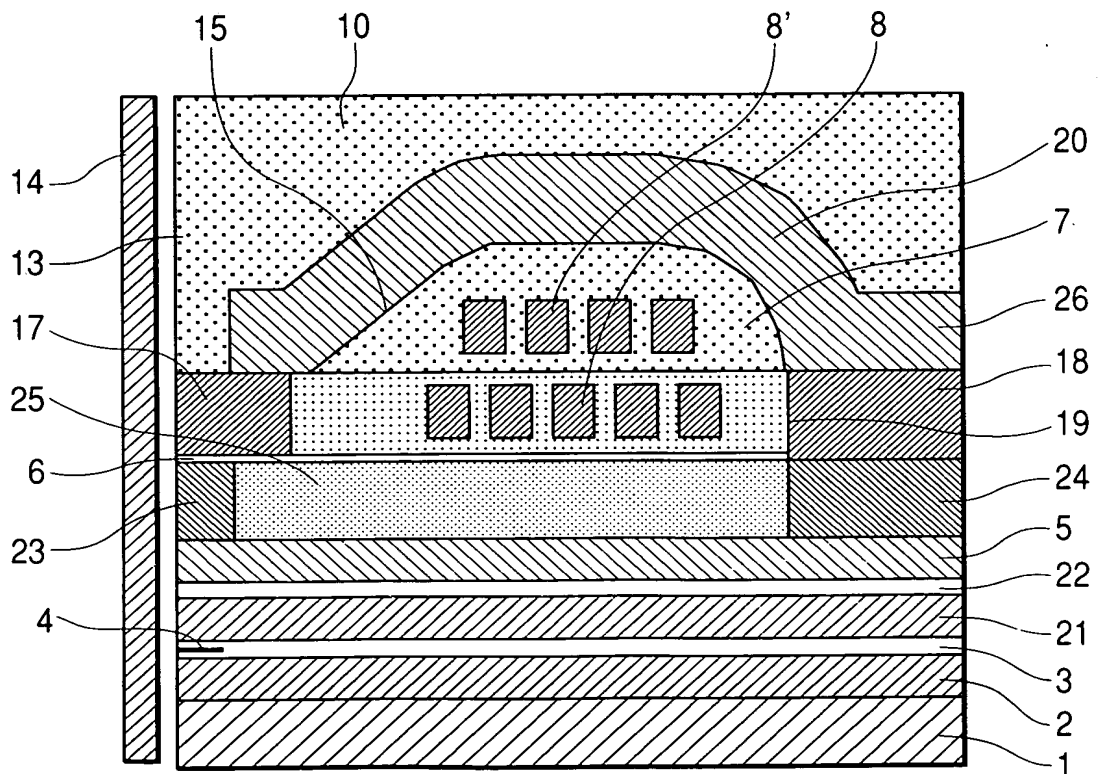


FIG. 3

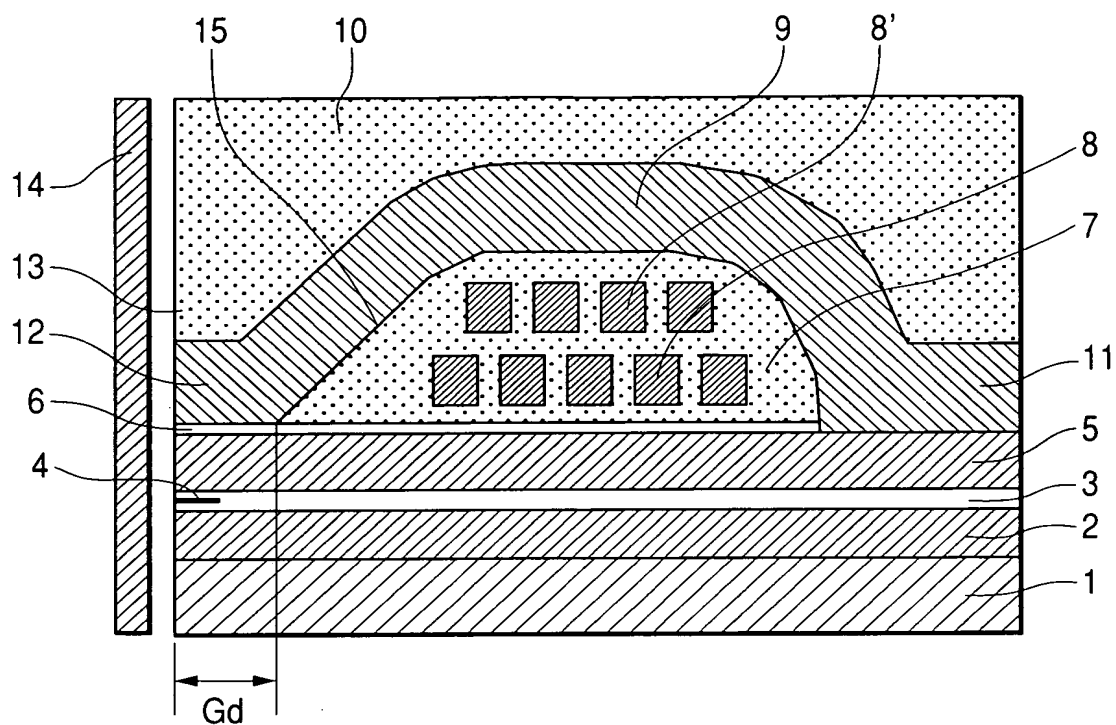
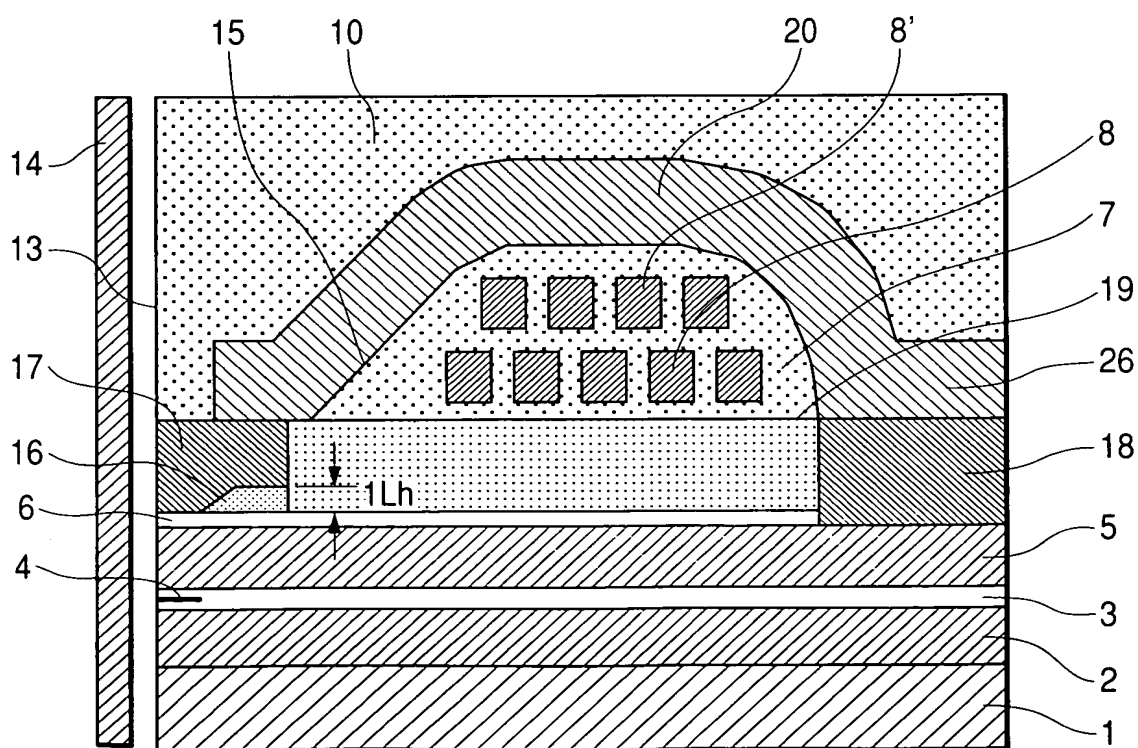
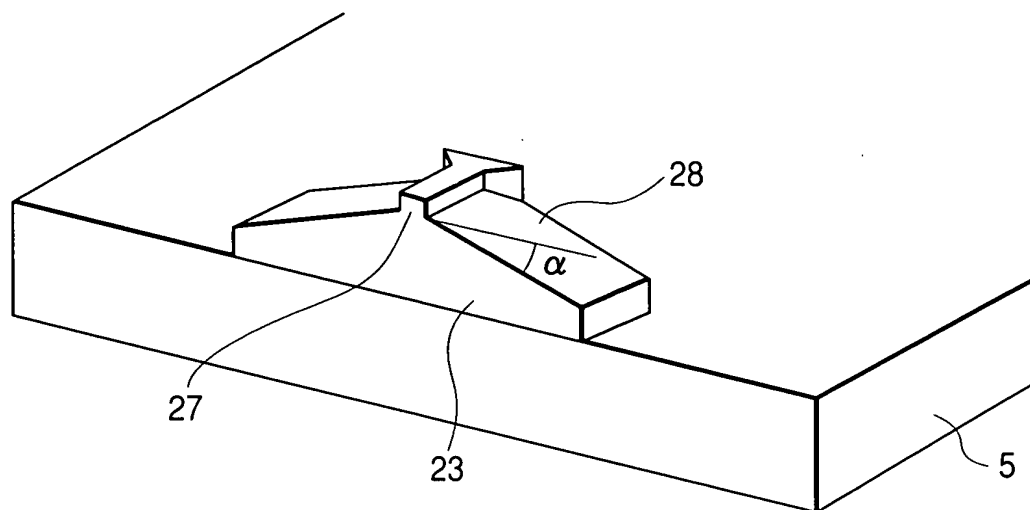


FIG. 4



*FIG. 5(a)*



*FIG. 5(b)*

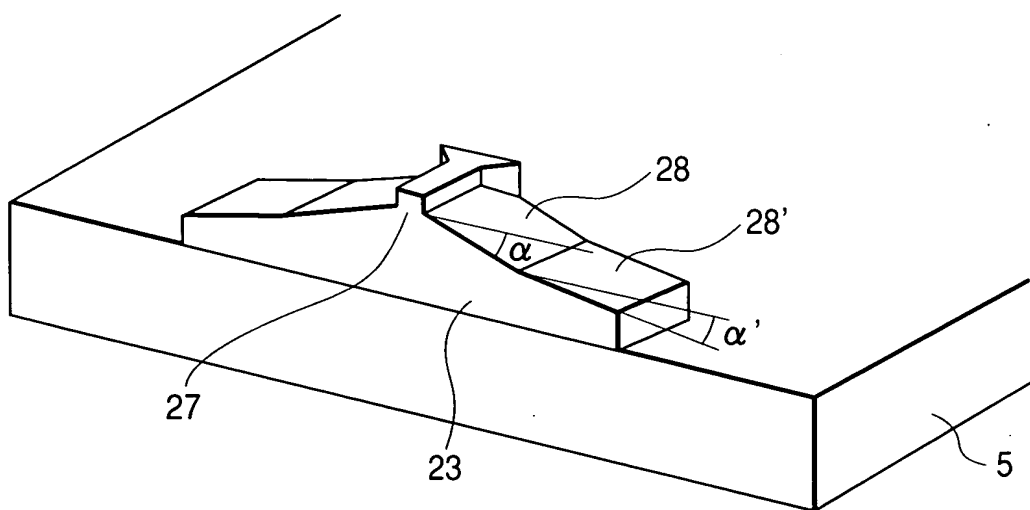


FIG. 5(a)

FIG. 6

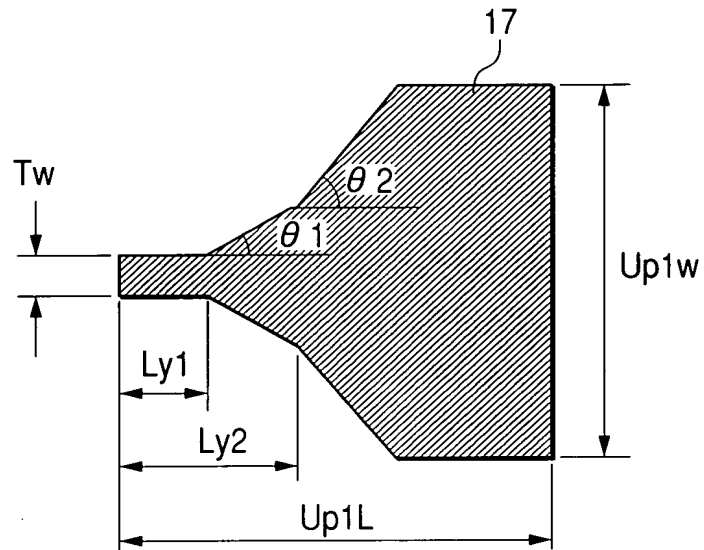
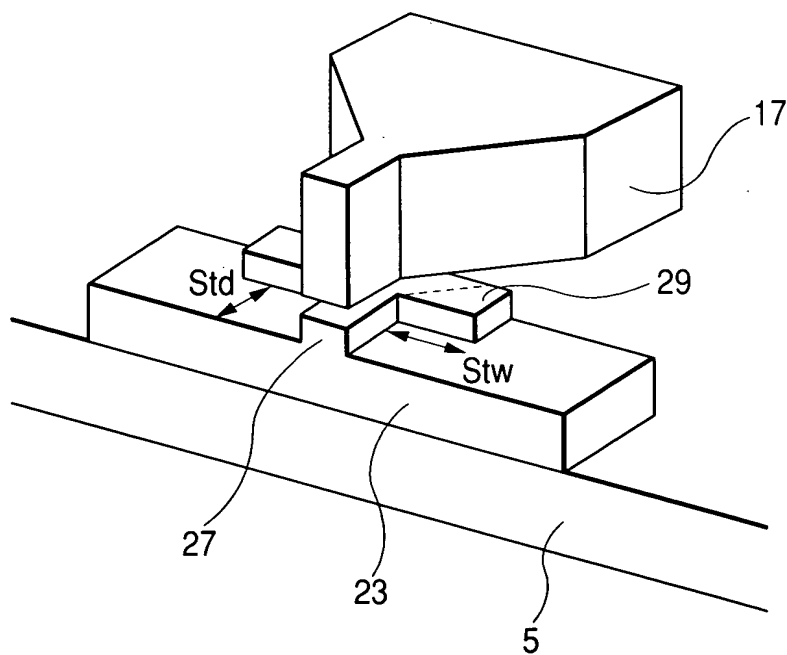
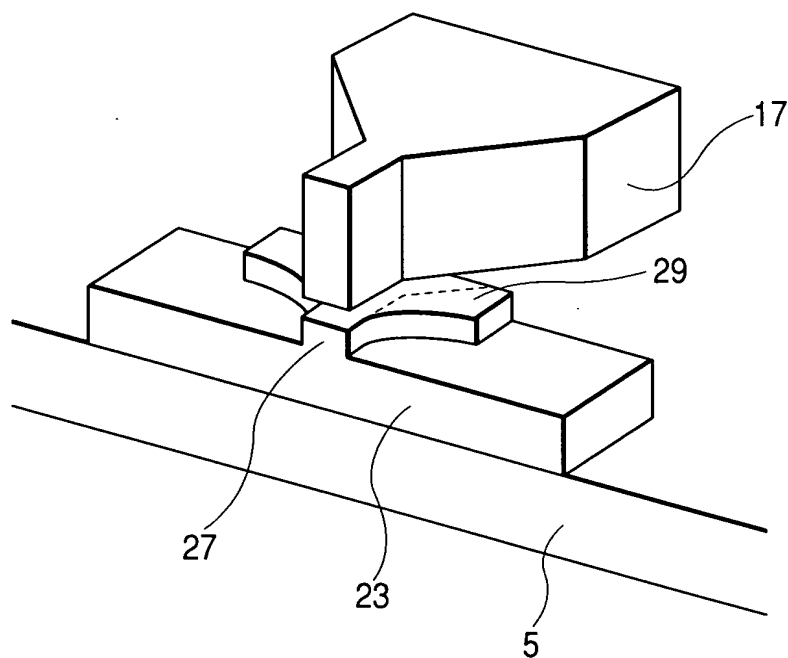


FIG. 7



**FIG. 8(a)**



**FIG. 8(b)**

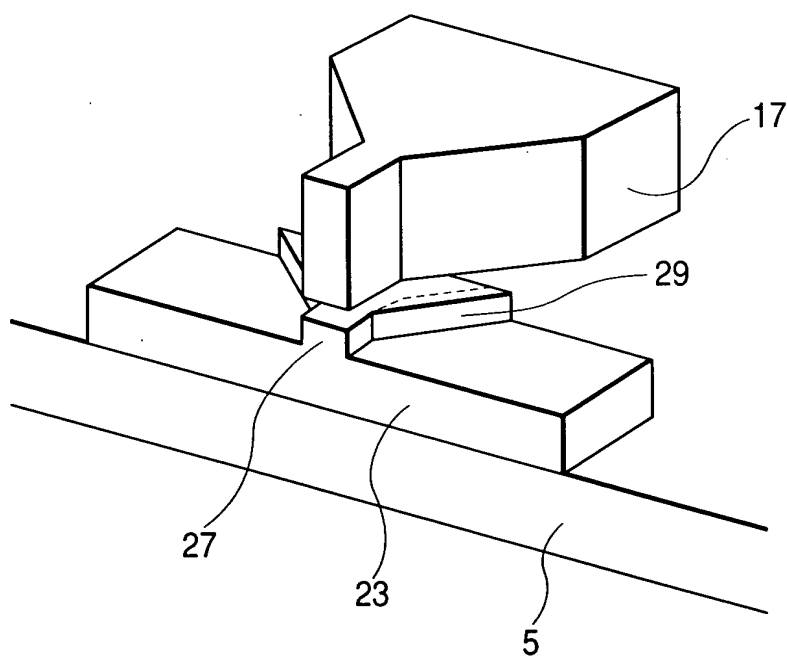


FIG. 8(a)

A detailed cross-sectional diagram of a semiconductor device structure. The diagram shows a stack of layers and components. At the bottom, there are several horizontal layers labeled 1, 2, 3, 21, 22, and 23. Above these is a layer labeled 4. A central region is defined by a layer labeled 6, which contains a series of small, shaded rectangular blocks. Above this central region is a layer labeled 25. The top of the structure is a large, curved, shaded region labeled 10, which is surrounded by a layer labeled 15. The entire structure is enclosed within a frame labeled 14. Other labels include 8, 8', 9, 11, and 24, which point to specific features and interfaces within the device.

FIG. 10(a)

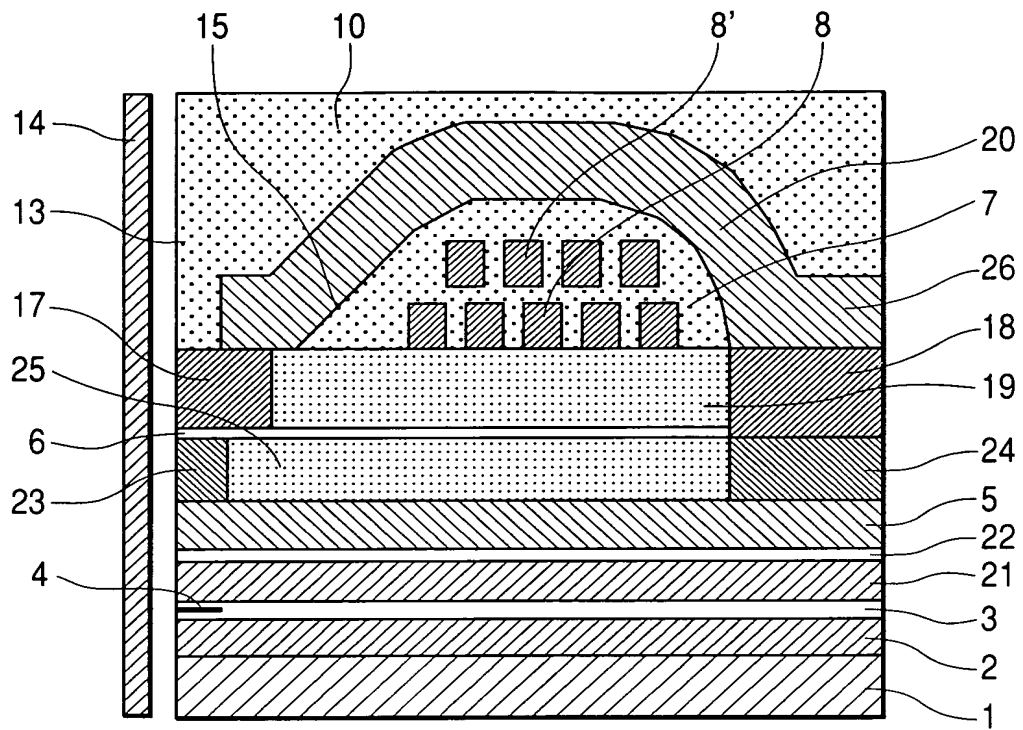
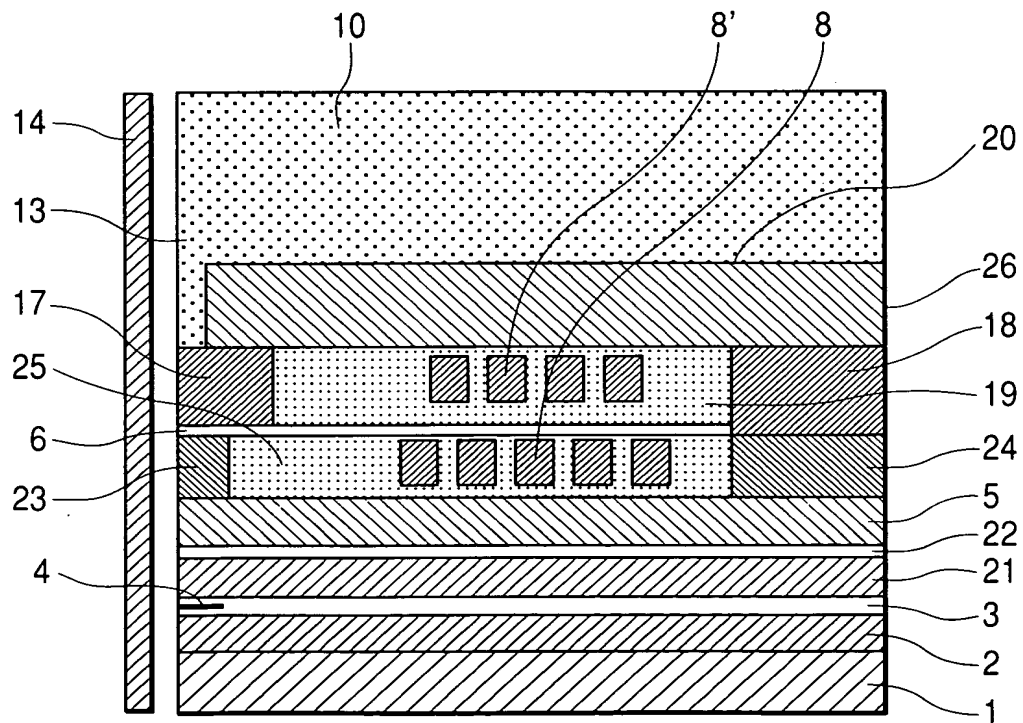
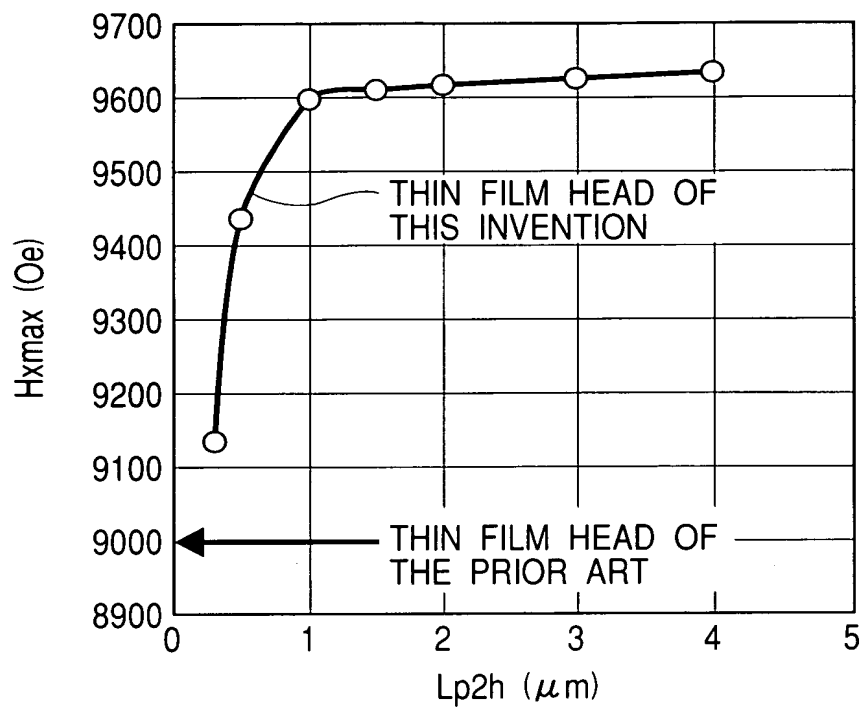
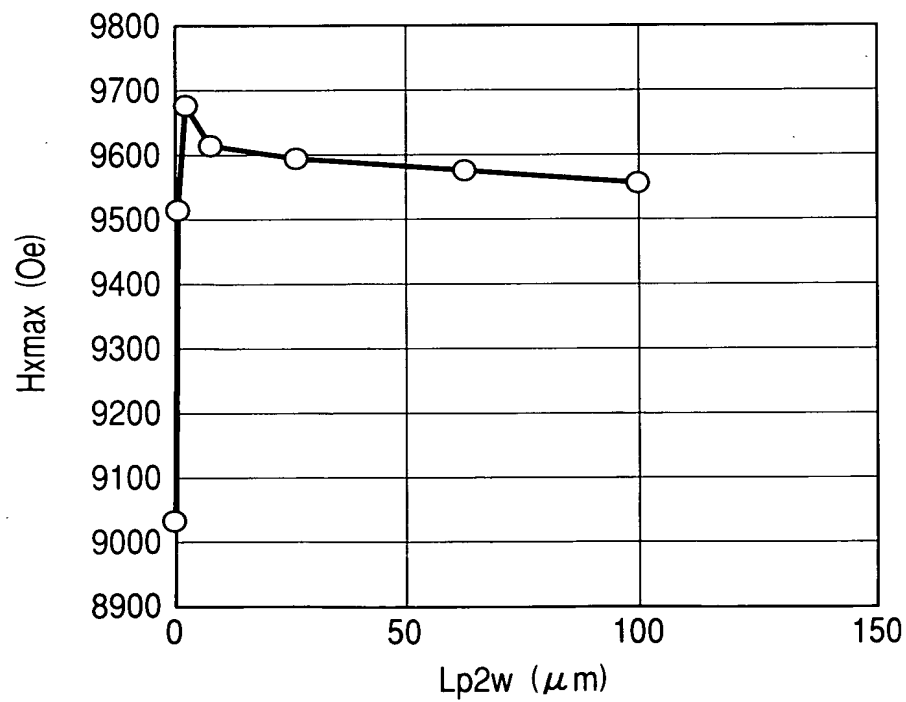


FIG. 10(b)

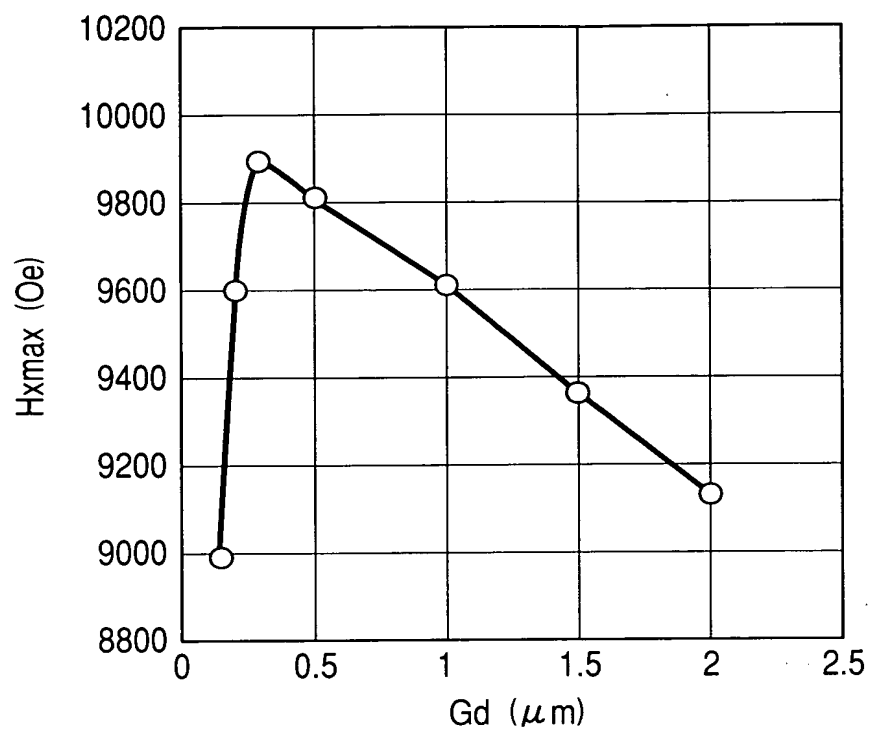


**FIG. 11****FIG. 12**

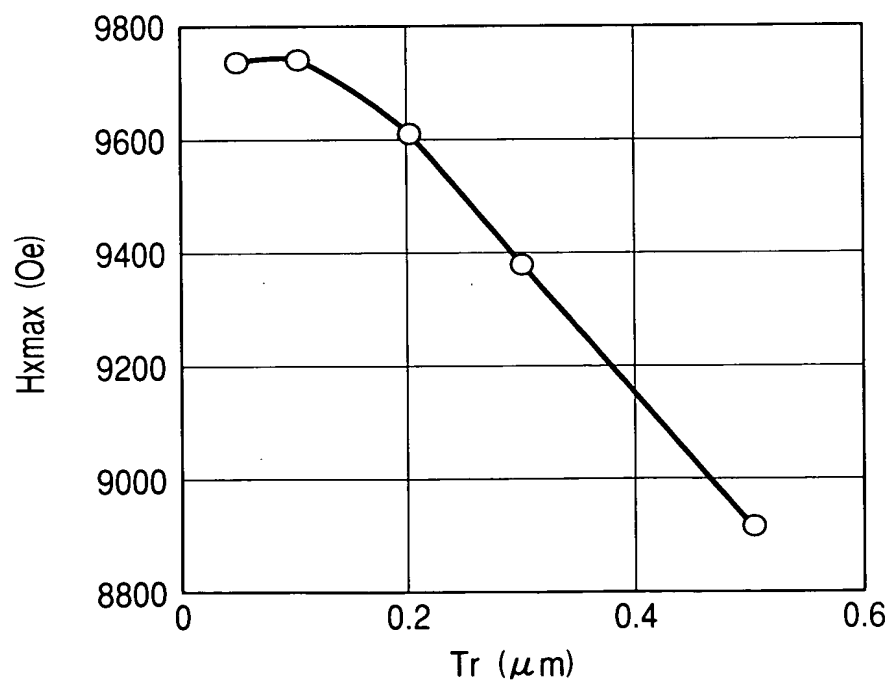


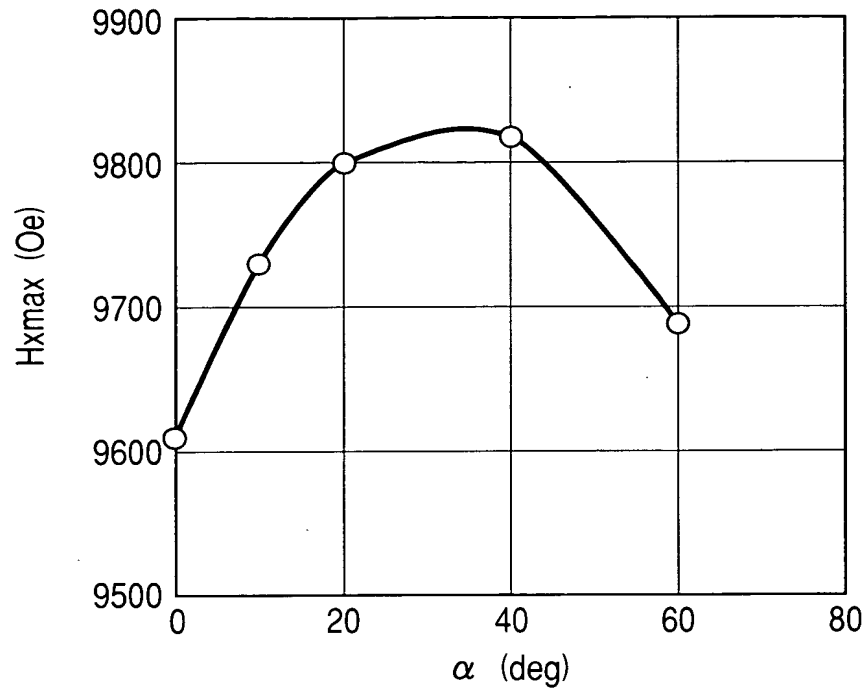
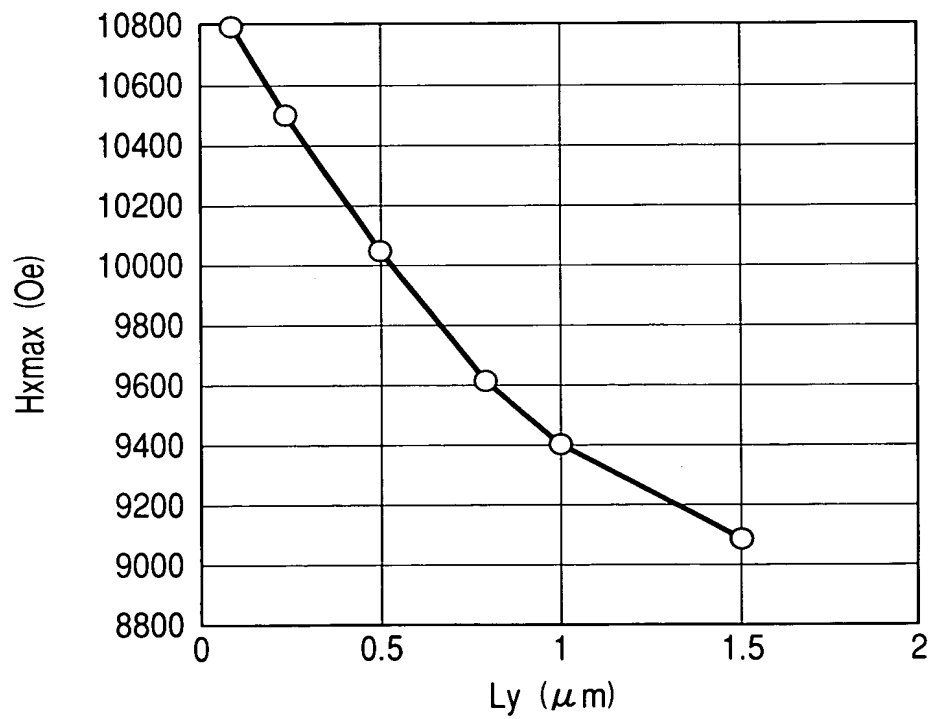
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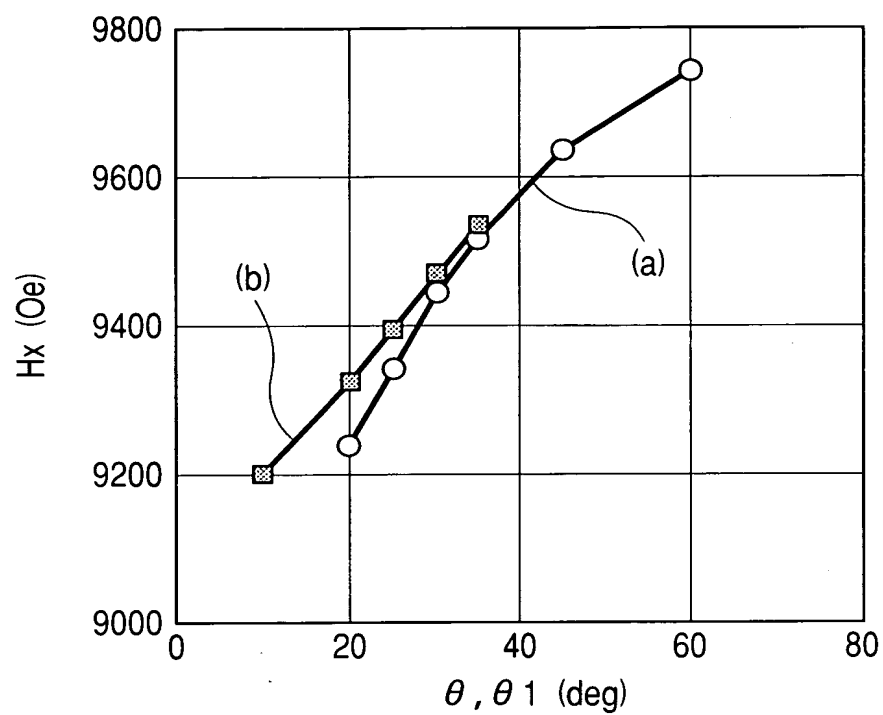
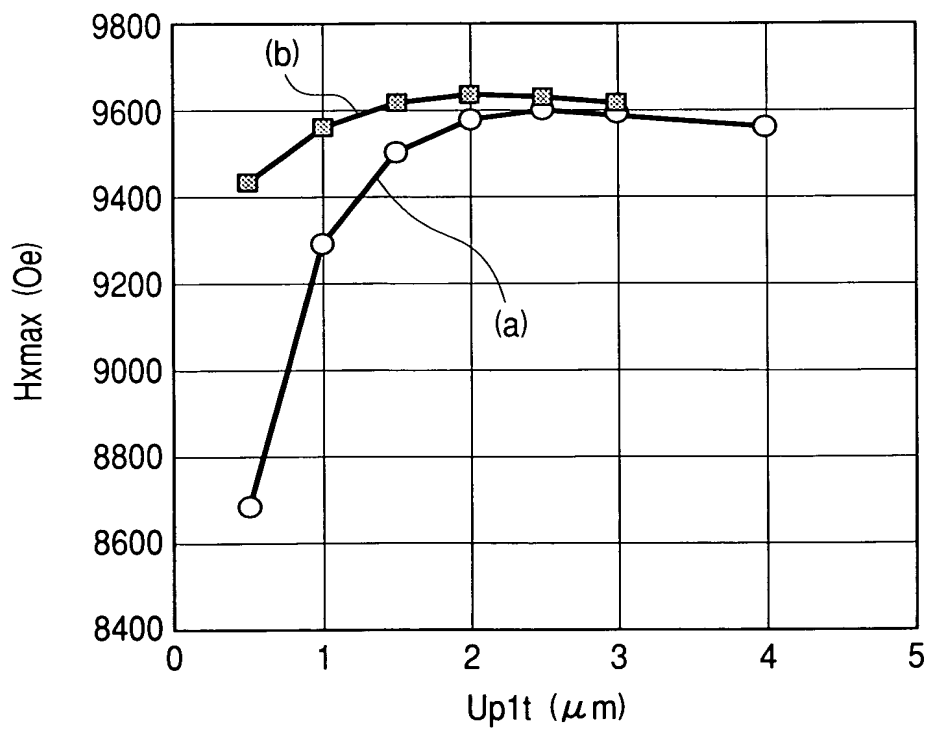
**FIG. 13**

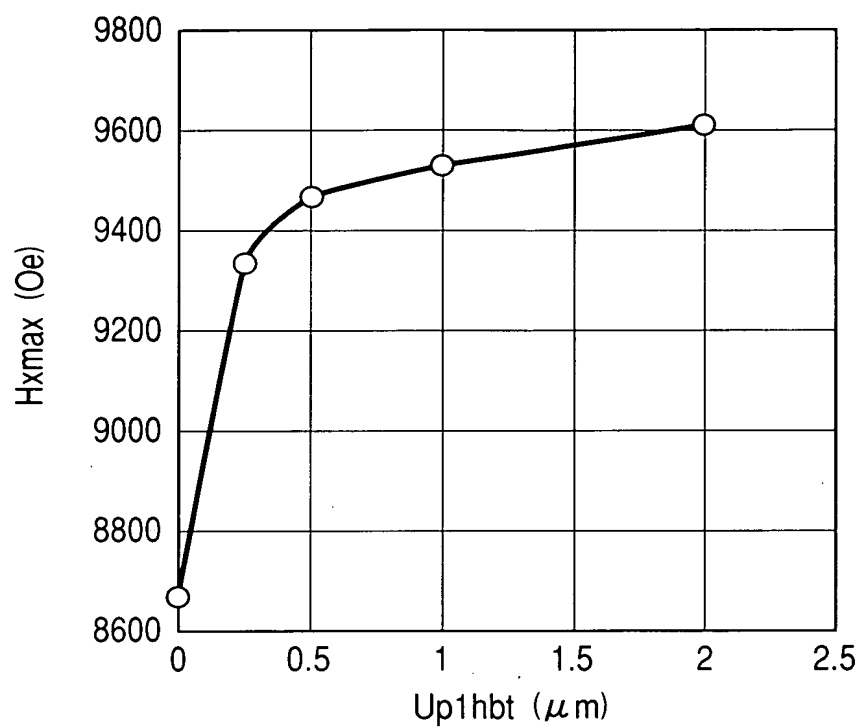
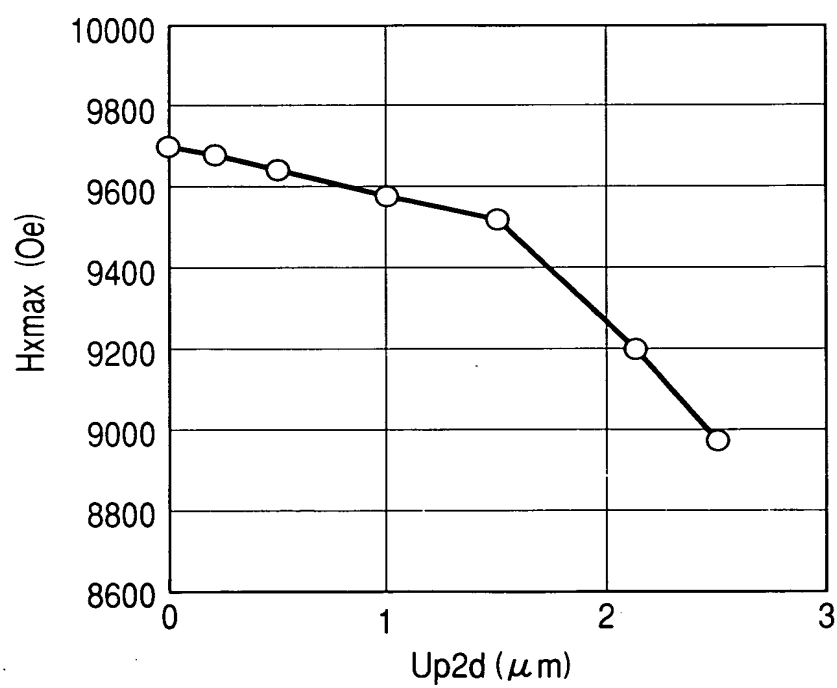


**FIG. 14**



*FIG. 15**FIG. 16*

**FIG. 17****FIG. 18**

*FIG. 19**FIG. 20*

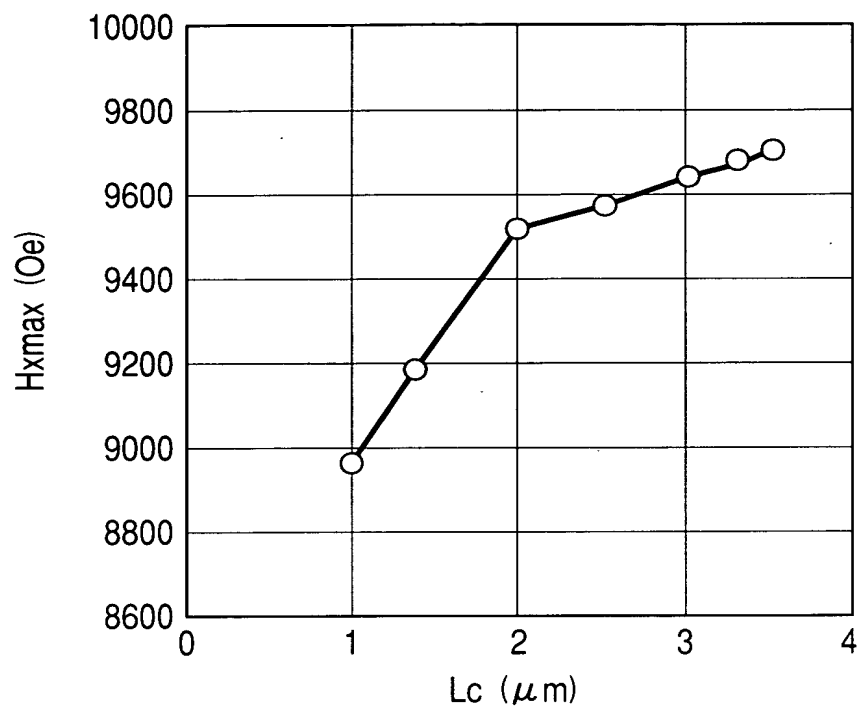
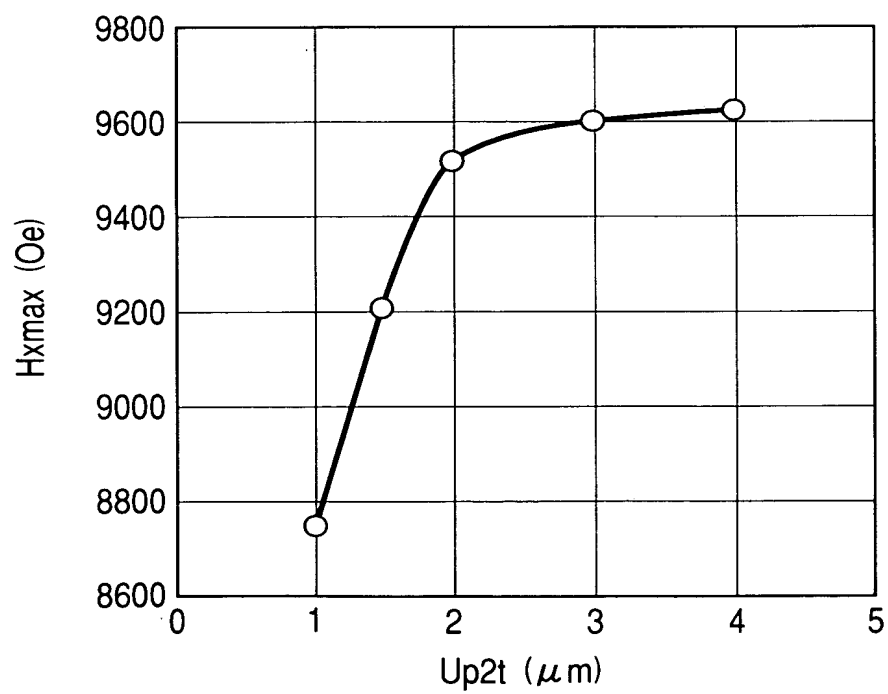
*FIG. 21**FIG. 22*

FIG. 23

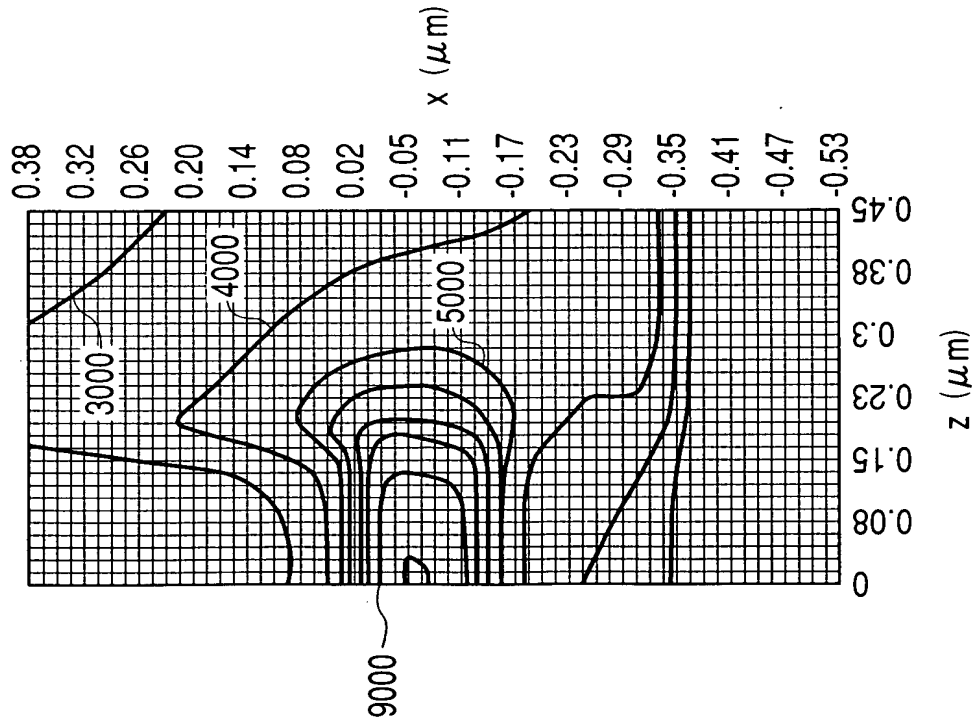
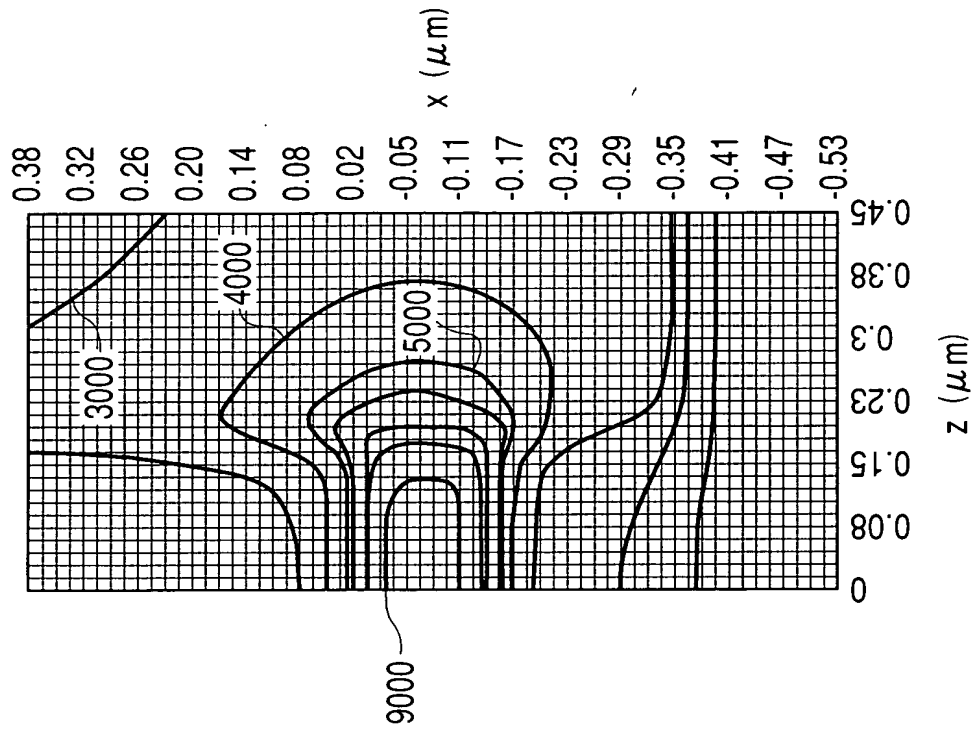
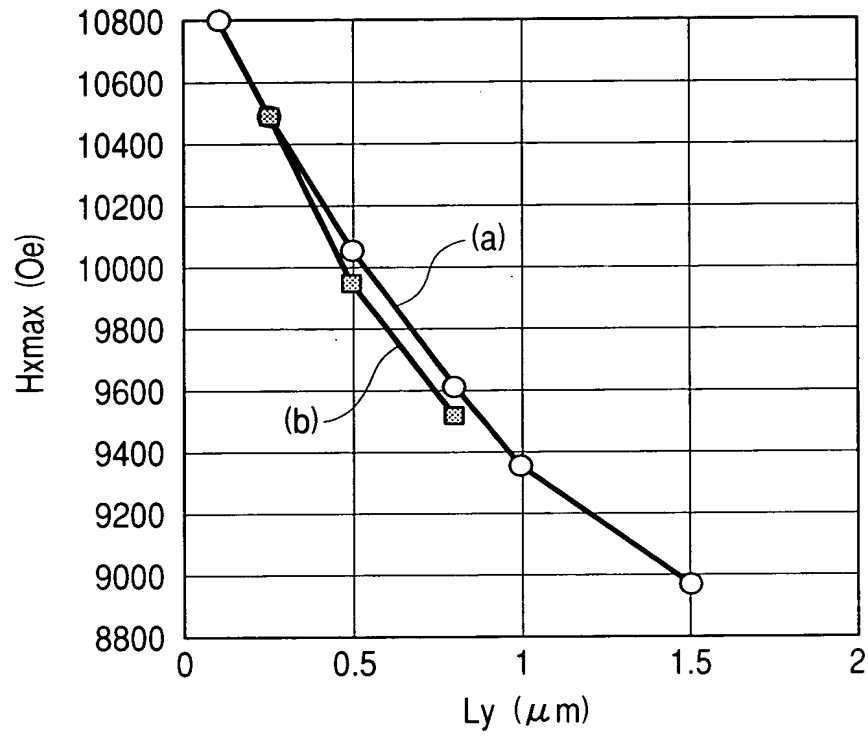
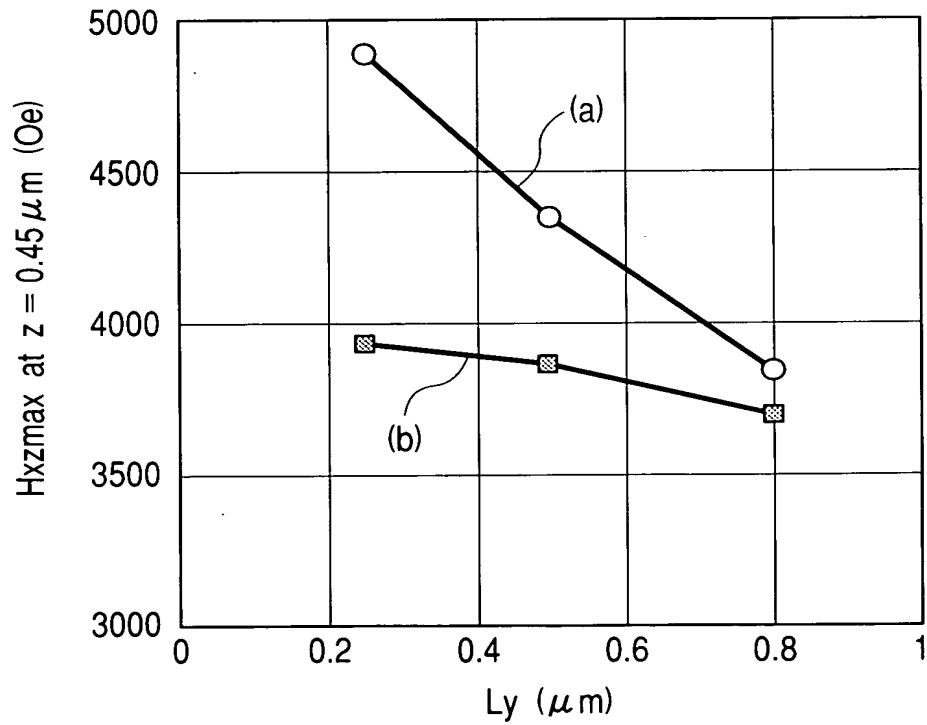
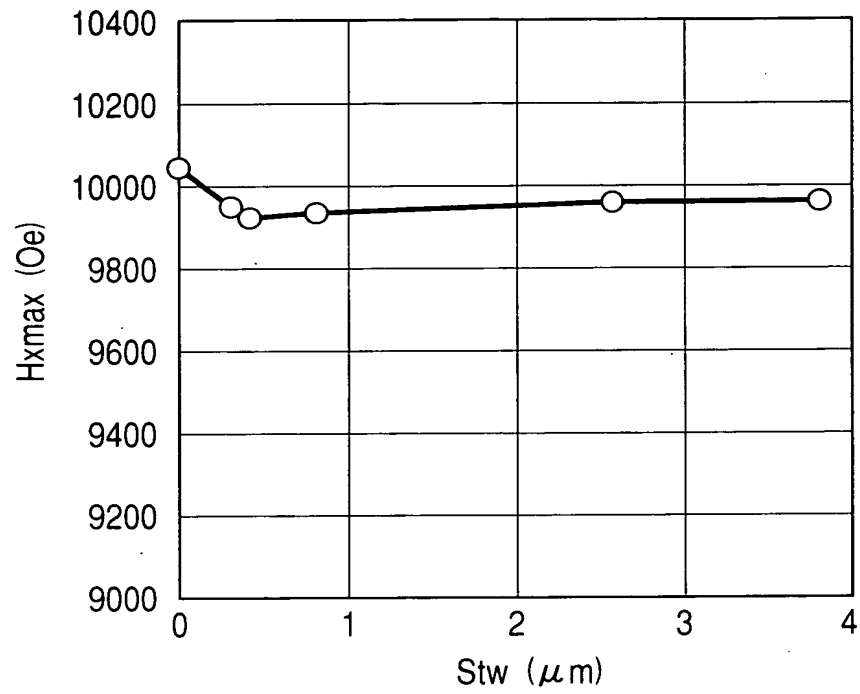
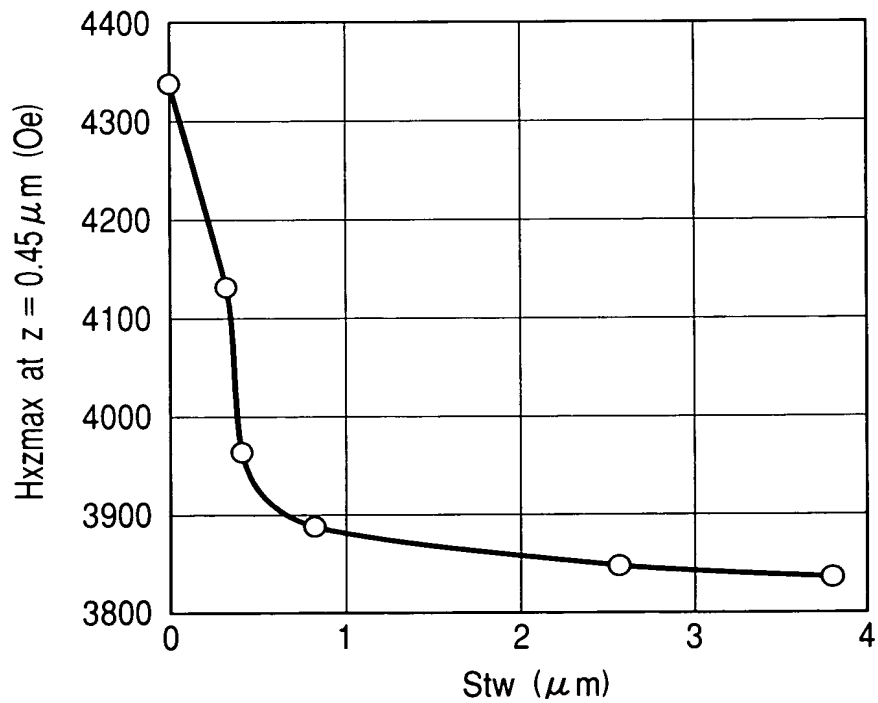


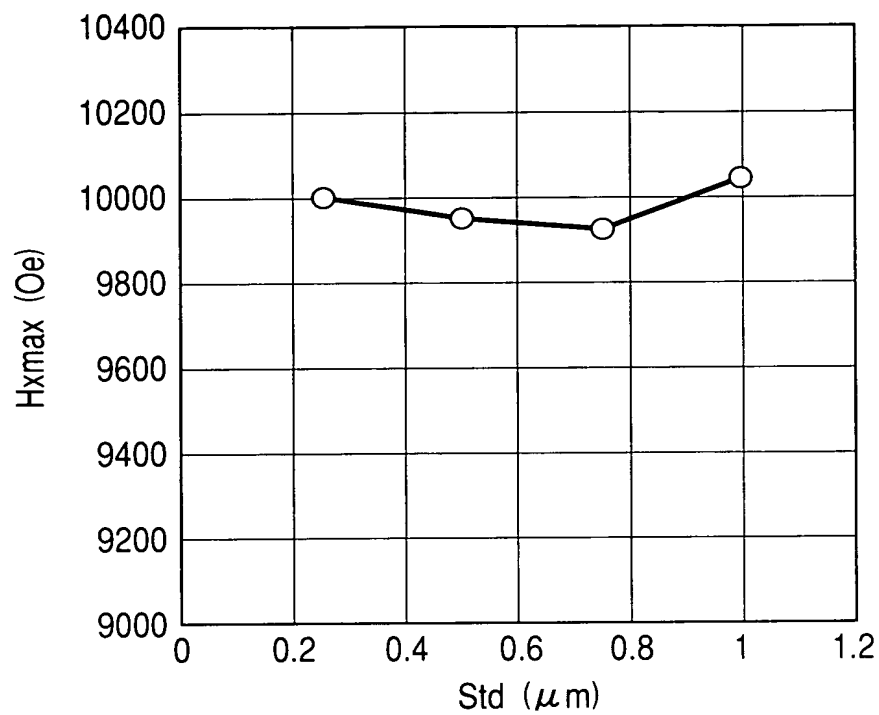
FIG. 24



**FIG. 25****FIG. 26**

*FIG. 27**FIG. 28*



*FIG. 29**FIG. 30*